



60N06

Power MOSFET

60 Amps, 60 Volts N-CHANNEL POWER MOSFET

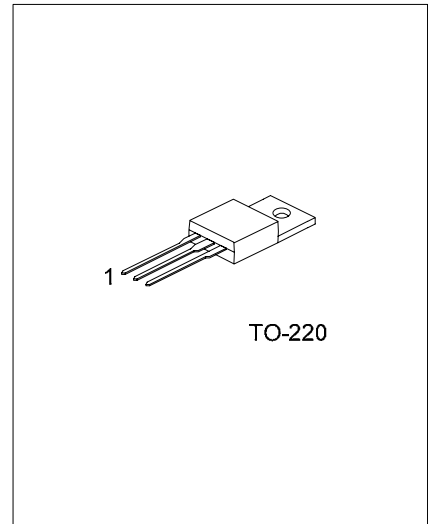
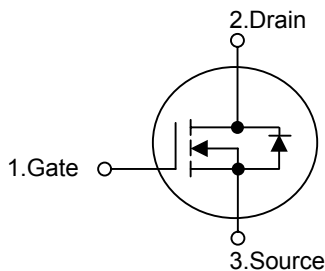
DESCRIPTION

The UTC **60N06** is n-channel enhancement mode power field effect transistors with stable off-state characteristics, fast switching speed, low thermal resistance, usually used at telecom and computer application.

FEATURES

- * $R_{DS(ON)} = 18m\Omega @ V_{GS} = 10 V$
- * Ultra low gate charge (typical 39 nC)
- * Fast switching capability
- * Low reverse transfer Capacitance ($C_{RSS} =$ typical 115 pF)
- * Avalanche energy Specified
- * Improved dv/dt capability, high ruggedness

SYMBOL



*Pb-free plating product number: 60N06L

ORDERING INFORMATION

Ordering Number		Package	Pin Assignment			Packing
Normal	Lead Free Plating		1	2	3	
60N06-TA3-T	60N06L-TA3-T	TO-220	G	D	S	Tube

Note: Pin Assignment: G: Gate D: Drain S: Source

<p>60N06L-TA3-T</p> <p>(1)Packing Type (2)Package Type (3)Lead Plating</p>	<p>(1) T: Tube, R: Tape Reel (2) TA3: TO-220 (3) L: Lead Free Plating, Blank: Pb/Sn</p>
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■ ABSOLUTE MAXIMUM RATINGS

PARAMETER	SYMBOL	RATINGS	UNIT	
Drain to Source Voltage	V_{DSS}	60	V	
Gate to Source Voltage	V_{GS}	± 20	V	
Continuous Drain Current	I_D	$T_C = 25$	60	A
		$T_C = 100$	39	A
Drain Current Pulsed (Note 1)	I_{DM}	120	A	
Avalanche Energy	E_{AS}	Single Pulsed (Note 2)	1000	mJ
		Repetitive (Note 1)	180	mJ
Total Power Dissipation	P_D	120	W	
Junction Temperature	T_J	+175		
Storage Temperature	T_{STG}	-55 ~ +175		

Note: Absolute maximum ratings are those values beyond which the device could be permanently damaged. Absolute maximum ratings are stress ratings only and functional device operation is not implied.

■ THERMAL DATA

PARAMETER	SYMBOL	MIN	TYP	MAX	UNIT
Thermal Resistance Junction-Ambient	θ_{JA}			62.5	/W
Thermal Resistance Junction-Case	θ_{JC}			1.25	/W

■ ELECTRICAL CHARACTERISTICS ($T_C = 25$, unless otherwise specified)

PARAMETER	SYMBOL	TEST CONDITIONS	MIN	TYP	MAX	UNIT
OFF CHARACTERISTICS						
Drain-Source Breakdown Voltage	BV_{DSS}	$V_{GS} = 0\text{ V}, I_D = 250\ \mu\text{A}$	60			V
Drain-Source Leakage Current	I_{DSS}	$V_{DS} = 60\text{ V}, V_{GS} = 0\text{ V}$			1	μA
Gate-Source Leakage Current	I_{GSS}	Forward $V_{GS} = 20\text{ V}, V_{DS} = 0\text{ V}$			100	nA
		Reverse $V_{GS} = -20\text{ V}, V_{DS} = 0\text{ V}$			-100	nA
ON CHARACTERISTICS						
Gate Threshold Voltage	$V_{GS(TH)}$	$V_{DS} = V_{GS}, I_D = 250\ \mu\text{A}$	2.0		4.0	V
Static Drain-Source On-State Resistance	$R_{DS(ON)}$	$V_{GS} = 10\text{ V}, I_D = 30\text{ A}$		14	18	m Ω
DYNAMIC CHARACTERISTICS						
Input Capacitance	C_{ISS}	$V_{GS} = 0\text{ V}, V_{DS} = 25\text{ V}, f = 1\text{ MHz}$		2000		pF
Output Capacitance	C_{OSS}			400		pF
Reverse Transfer Capacitance	C_{RSS}			115		pF
SWITCHING CHARACTERISTICS						
Turn-On Delay Time	$t_{D(ON)}$	$V_{DD} = 30\text{ V}, I_D = 60\text{ A}, R_L = 0.5\ \Omega,$ $V_{GS} = 10\text{ V}$ (Note 4, 5)		12	30	ns
Rise Time	t_R			11	30	ns
Turn-Off Delay Time	$t_{D(OFF)}$			25	50	ns
Fall Time	t_F			15	30	ns
Total Gate Charge	Q_G	$V_{DS} = 30\text{ V}, V_{GS} = 10\text{ V}$ $I_D = 60\text{ A}$ (Note 4, 5)		39	60	nC
Gate-Source Charge	Q_{GS}			12		nC
Gate-Drain Charge (Miller Charge)	Q_{GD}			10		nC

■ ELECTRICAL CHARACTERISTICS(Cont.)

PARAMETER	SYMBOL	TEST CONDITIONS	MIN	TYP	MAX	UNIT
SOURCE-DRAIN DIODE RATINGS AND CHARACTERISTICS						
Diode Forward Voltage	V_{SD}	$V_{GS} = 0\text{ V}, I_S = 60\text{ A}$			1.6	V
Continuous Source Current	I_S				60	A
Pulsed Source Current	I_{SM}				120	
Reverse Recovery Time	t_{RR}	$I_S = 60\text{ A}, V_{GS} = 0\text{ V},$ $di_F / dt = 100\text{ A}/\mu\text{s}$		60		ns
Reverse Recovery Charge	Q_{RR}			3.4		μC

Note 1. Repeatability rating: pulse width limited by junction temperature

2. $L=0.61\text{mH}, I_{AS}=60\text{A}, R_G=20\Omega$, Starting $T_J=25$

3. $I_{SD}\leq 60\text{A}, di/dt\leq 300\text{A}/\mu\text{s}, V_{DD}\leq BV_{DSS}$, Starting $T_J=25$

4. Pulse Test: Pulse Width $\leq 300\mu\text{s}$, Duty Cycles $\leq 2\%$

5. Essentially independent of operating temperature.

■ TEST CIRCUITS AND WAVEFORMS

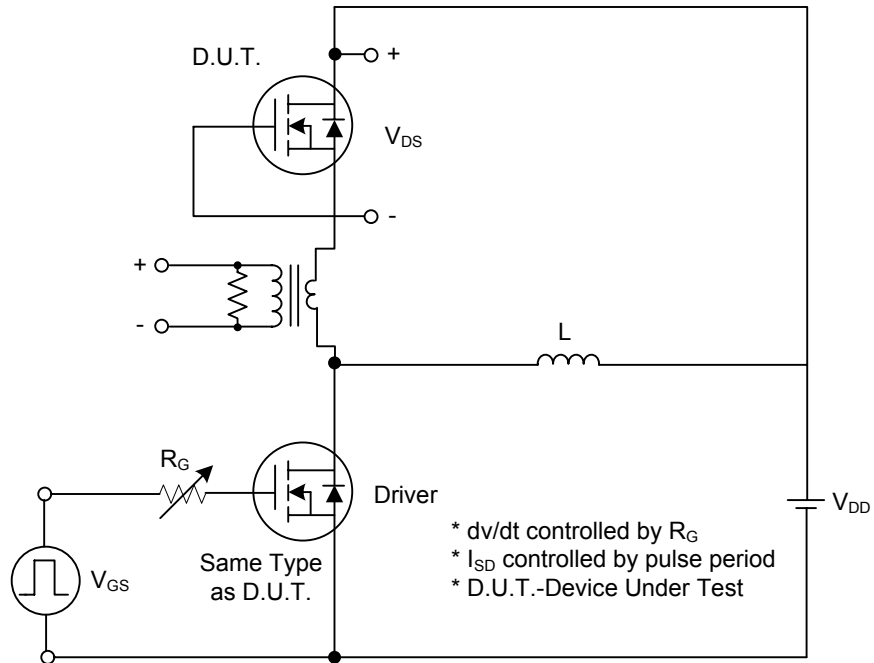


Fig. 1A Peak Diode Recovery dv/dt Test Circuit

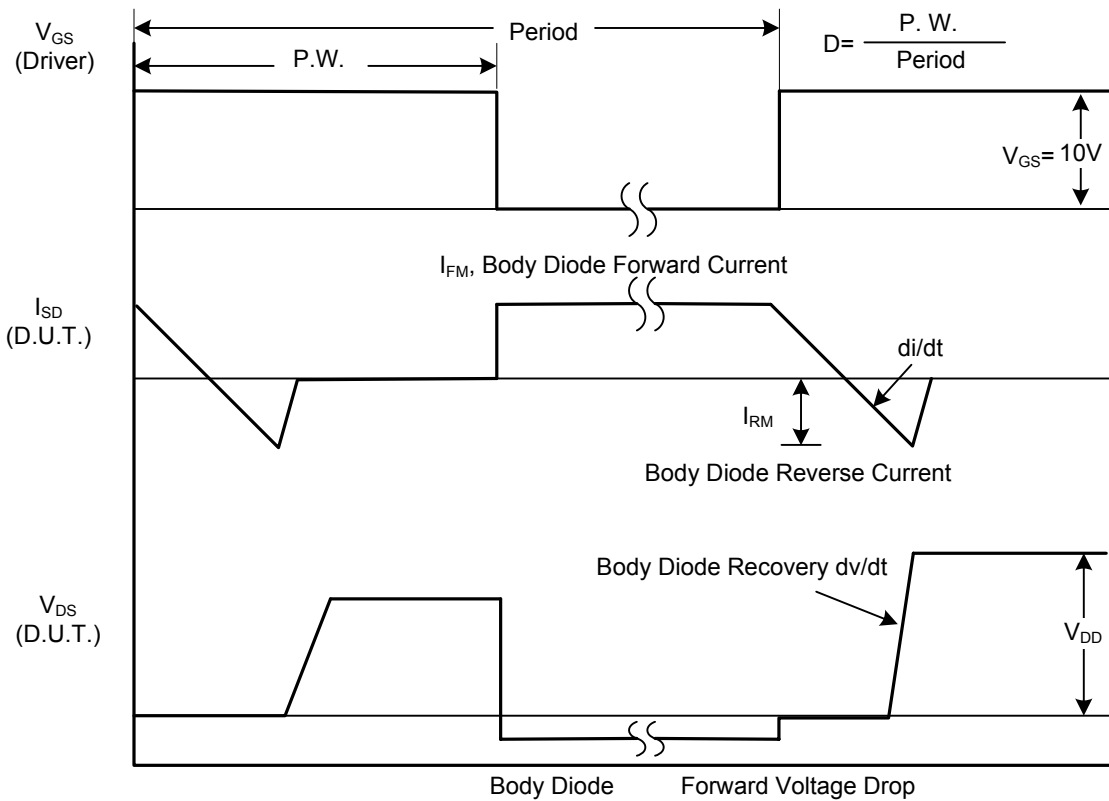


Fig. 1B Peak Diode Recovery dv/dt Waveforms

■ TEST CIRCUITS AND WAVEFORMS (Cont.)

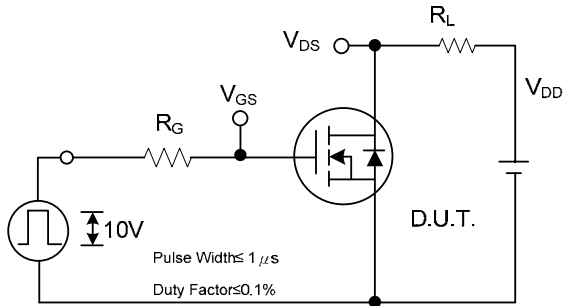


Fig. 2A Switching Test Circuit

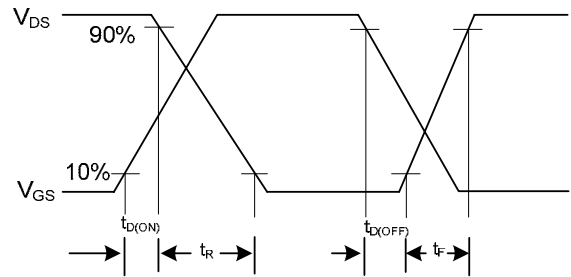


Fig. 2B Switching Waveforms

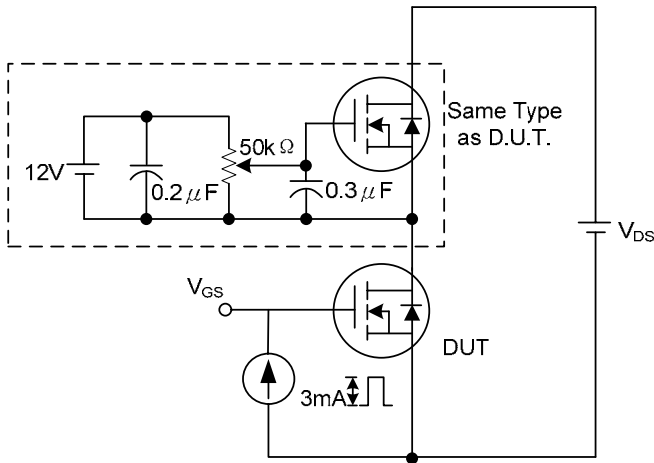


Fig. 3A Gate Charge Test Circuit

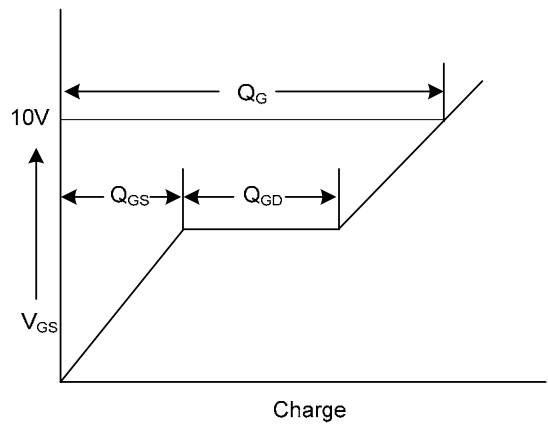


Fig. 3B Gate Charge Waveform

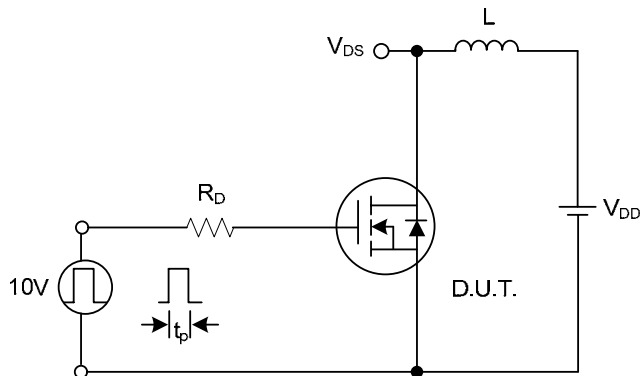


Fig. 4A Unclamped Inductive Switching Test Circuit

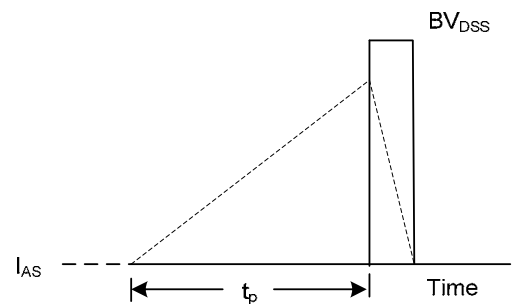
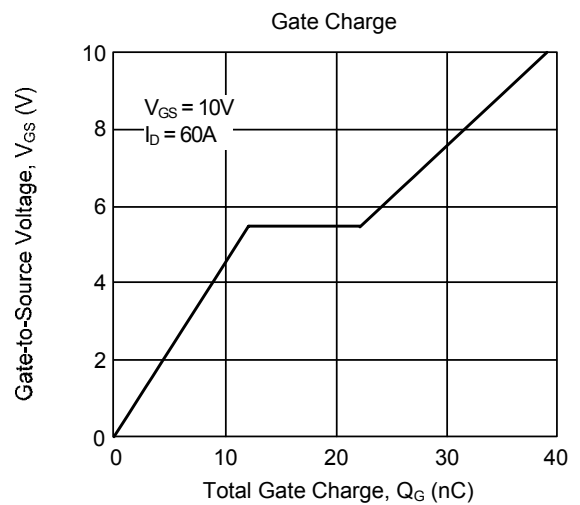
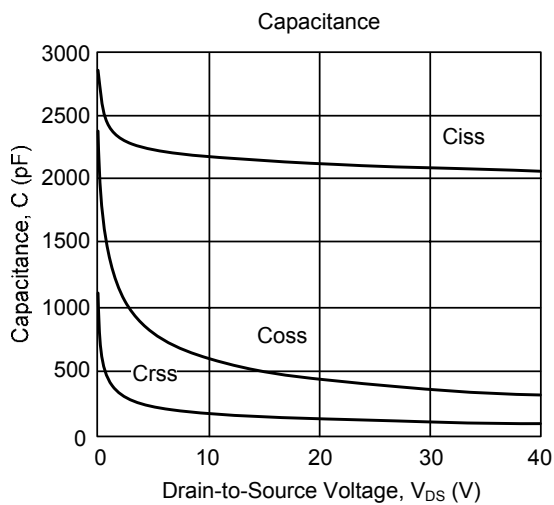
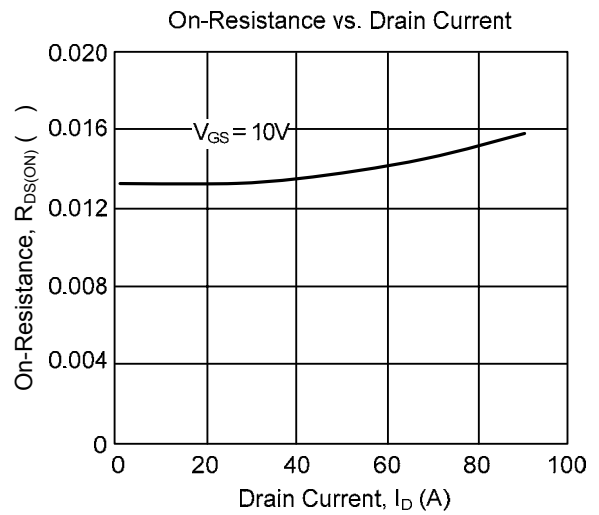
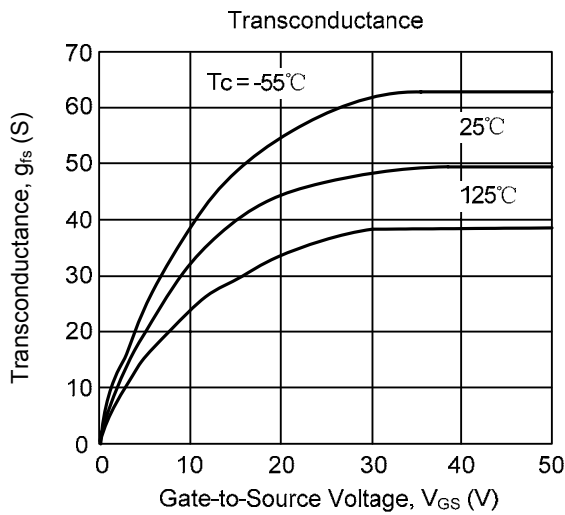
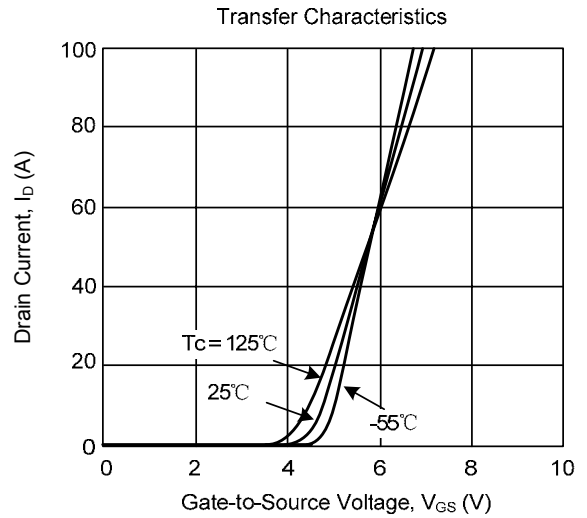
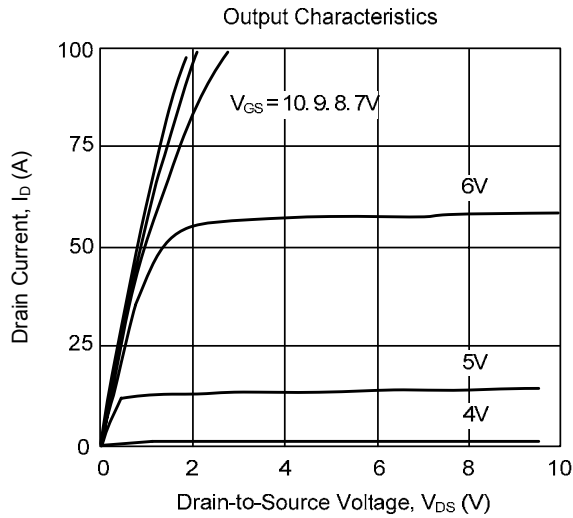
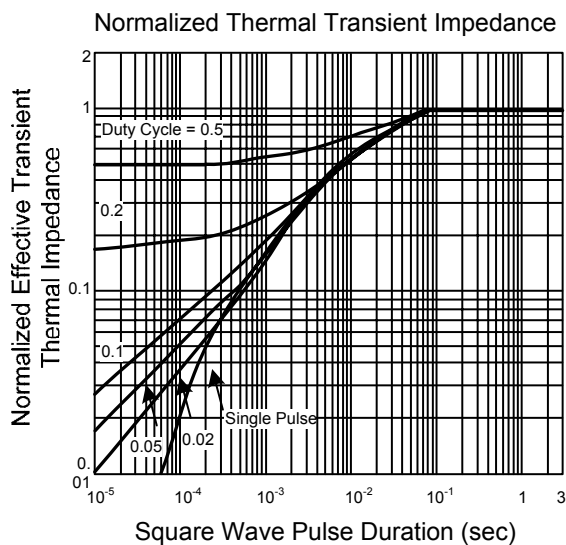
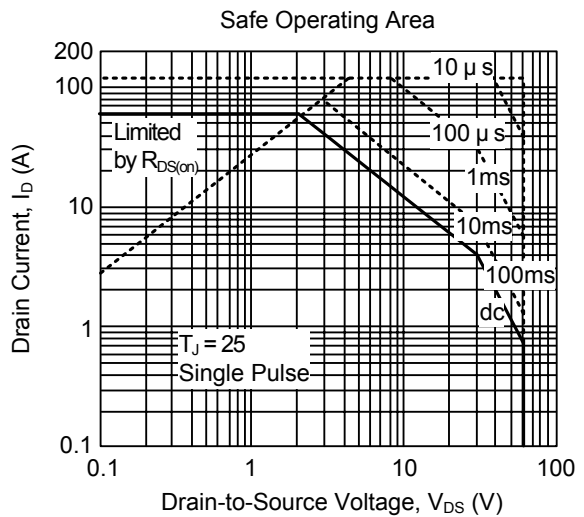
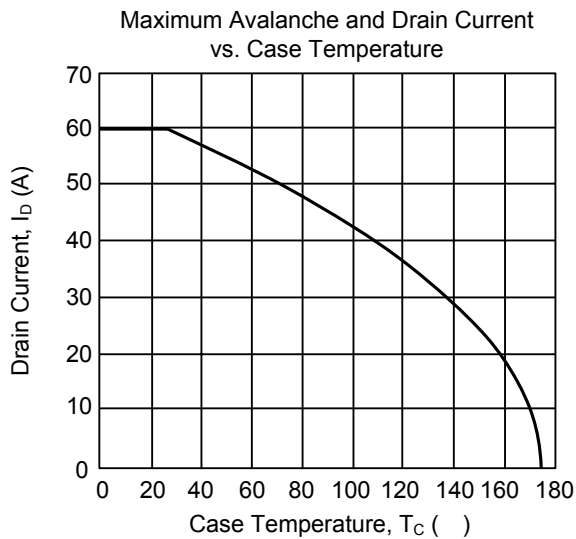
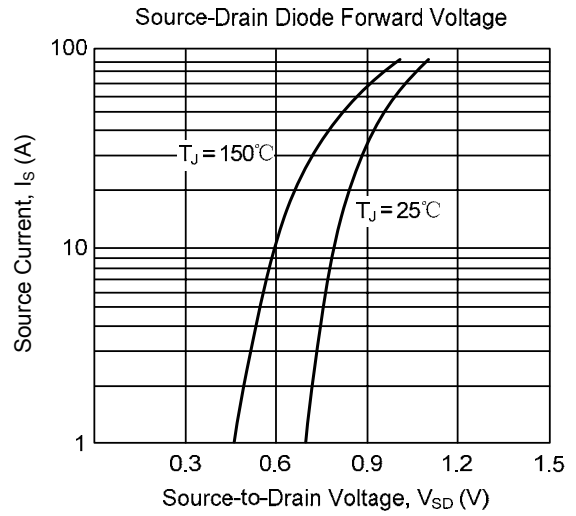
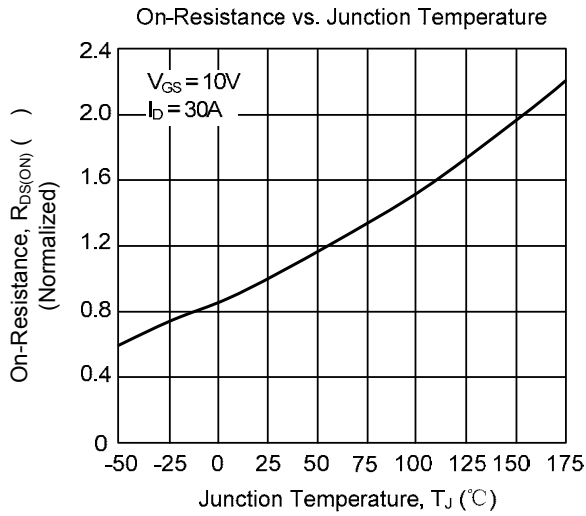


Fig. 4B Unclamped Inductive Switching Waveforms

■ TYPICAL CHARACTERISTICS



TYPICAL CHARACTERISTICS(Cont.)



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